Parallel Programming and Optimization with Intel® Xeon® and Xeon Phi™ Platforms

Intel is offering an updated and expanded series of software developer trainings in parallel programming using the Intel® Xeon® and Xeon Phi™ platforms

This training seminar provides software developers the foundation needed for modernizing their codes to extract more of the parallel compute performance potential found in Intel® Xeon® and Intel® Xeon Phi™ platforms, including Intel's next-generation Xeon Phi™ processor, Knights Landing.

The course contains materials and practical exercises appropriate for developers beginning their journey to parallel programming, as well as provide cutting-edge detail to HPC experts on the best practices for Intel's multicore and many-core architectures and software development tools. This offering includes a free one-day hybrid introductory seminar and hands-on laboratory.

The training targets software engineers and architects, and covers the following topics:

- Intel Xeon Phi™ architecture: purpose, organization, pre-requisites for good performance, future technology
- Programming models: native, offload, heterogeneous clustering
- Parallel frameworks: automatic vectorization, OpenMP, MPI
- Optimization methods: general, scalar math, vectorization, multithreading, memory access, communication and special topics
- Knights Landing programming model: Introductory

For more information and workshop registration please visit:
http://tinyurl.com/2016RiceUniversity

Event Details: Hybrid Session
Date: March 1, 2016
Registration: 9:00 AM
Presentation: 9:30 AM to 4:00 PM
Location: Rice University
Bioscience Research Collaborative
2nd Floor Lecture Hall—Room 280
6500 Main Street
Houston, TX 77005

TRAININGS PRESENTED BY:

Sponsored by: intel

Executed by: COLFAX Customized Solutions

TRAININGS HOSTED BY:

RICE

Co-hosted by the Ken Kennedy Institute for Information Technology and the Center for Research Computing at Rice University