

FROM SCALAR & SERIAL TO VECTOR & PARALLEL

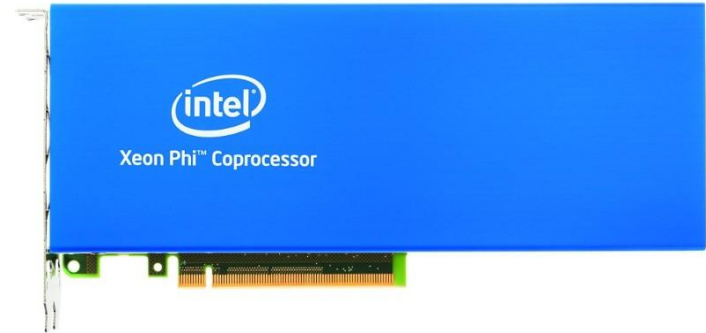
Hands-on Lab

Part 1 of 3

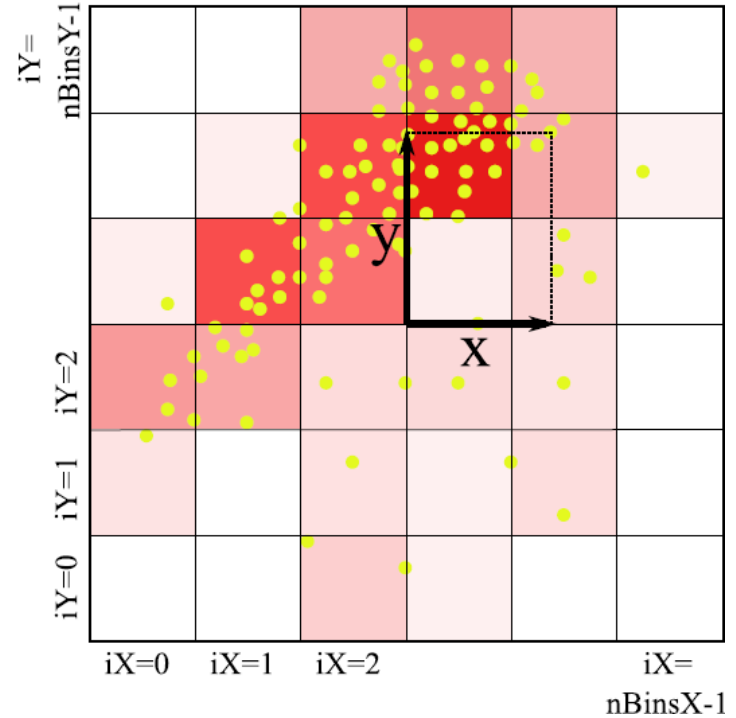
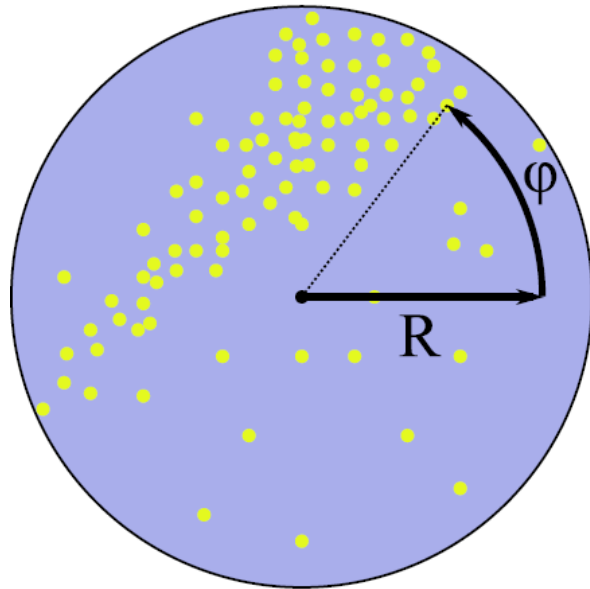


GOALS

- **Part 1: see multi-threading on Intel architecture in action**
- Part 2: learn to vectorize & future-proof vectorization
- Part 3: experiment with what it takes to make the memory subsystem happy

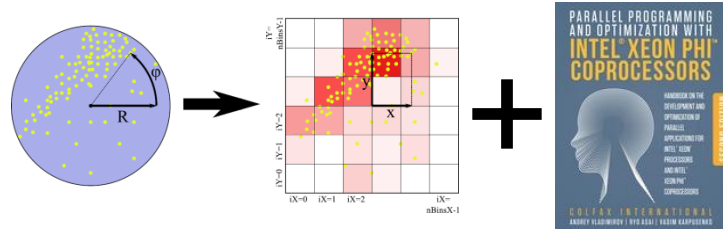


EXAMPLE PROBLEM: BINNING

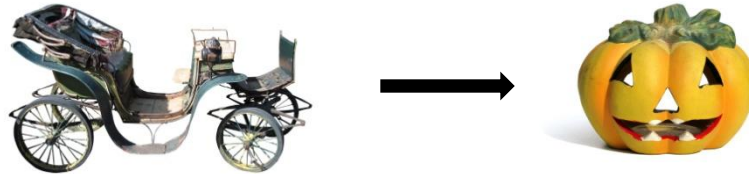


SERVER FOR EXERCISES

- Instructions at uni.colfax-intl.com/cdt
- Find code of lab + exercises from xeonphi.com/book



- Enjoy remote access until midnight



INITIAL APPROACH

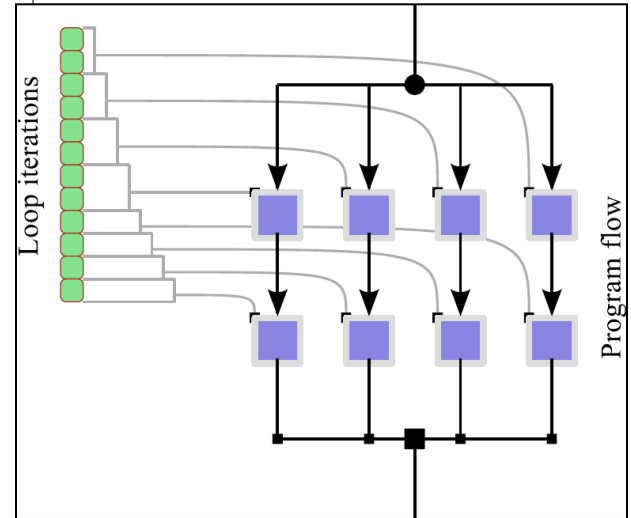
```
// Reference implementation: scalar, serial code without optimization
void BinParticlesReference(
    const InputDataType & inputData, BinsType & outputBins) {
    // Loop through all particle coordinates
    for (int i = 0; i < inputData.numDataPoints; i++) {
        // Transforming from cylindrical to Cartesian coordinates:
        const FTYPE x = inputData.r[i]*COS(inputData.phi[i]);
        const FTYPE y = inputData.r[i]*SIN(inputData.phi[i]);

        // Calculating the bin numbers for these coordinates:
        const int iX = int((x - xMin)*binsPerUnitX);
        const int iY = int((y - yMin)*binsPerUnitY);

        // Incrementing the appropriate bin in the counter:
        outputBins[iX][iY]++;
    }
}
```

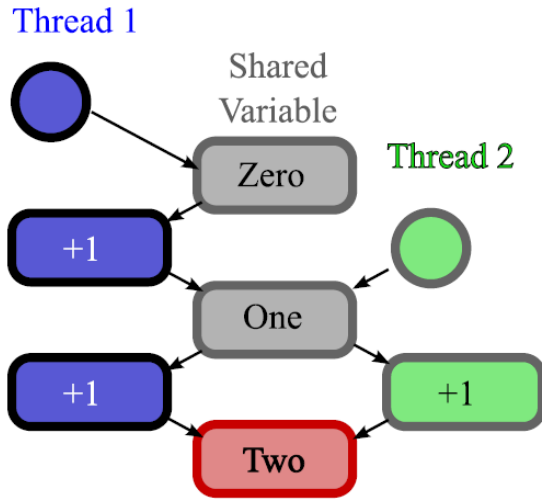
OPENMP THREADS

```
// Parallel, but INCORRECT implementation
void BinParticlesReference(
    const InputDataType & inputData,
    BinsType & outputBins) {
    // Distribute loop iterations across threads
    #pragma omp parallel for
    for (int i = 0; i < inputData.numDataPoints; i++)
    {
        // ...
        // Incrementing the appropriate
        // bin in the counter:
        outputBins[iX][iY]++;
    }
}
```

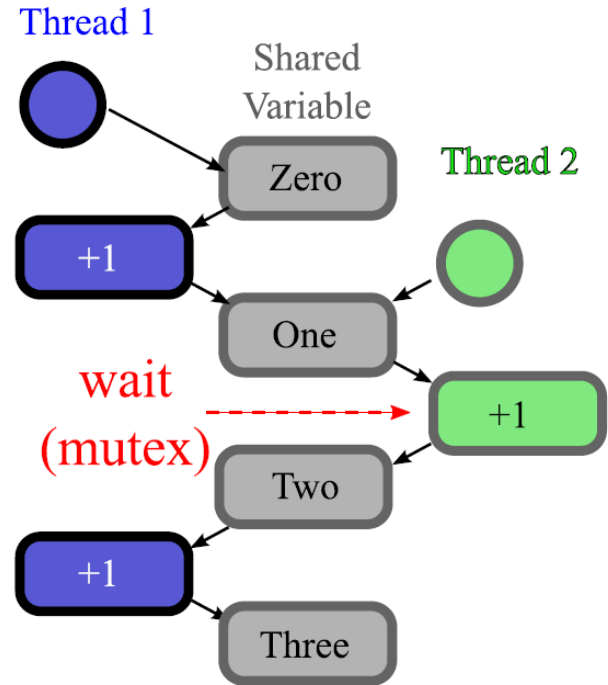


Software threads utilize logical processors in an Intel Xeon or an Intel Xeon Phi processor

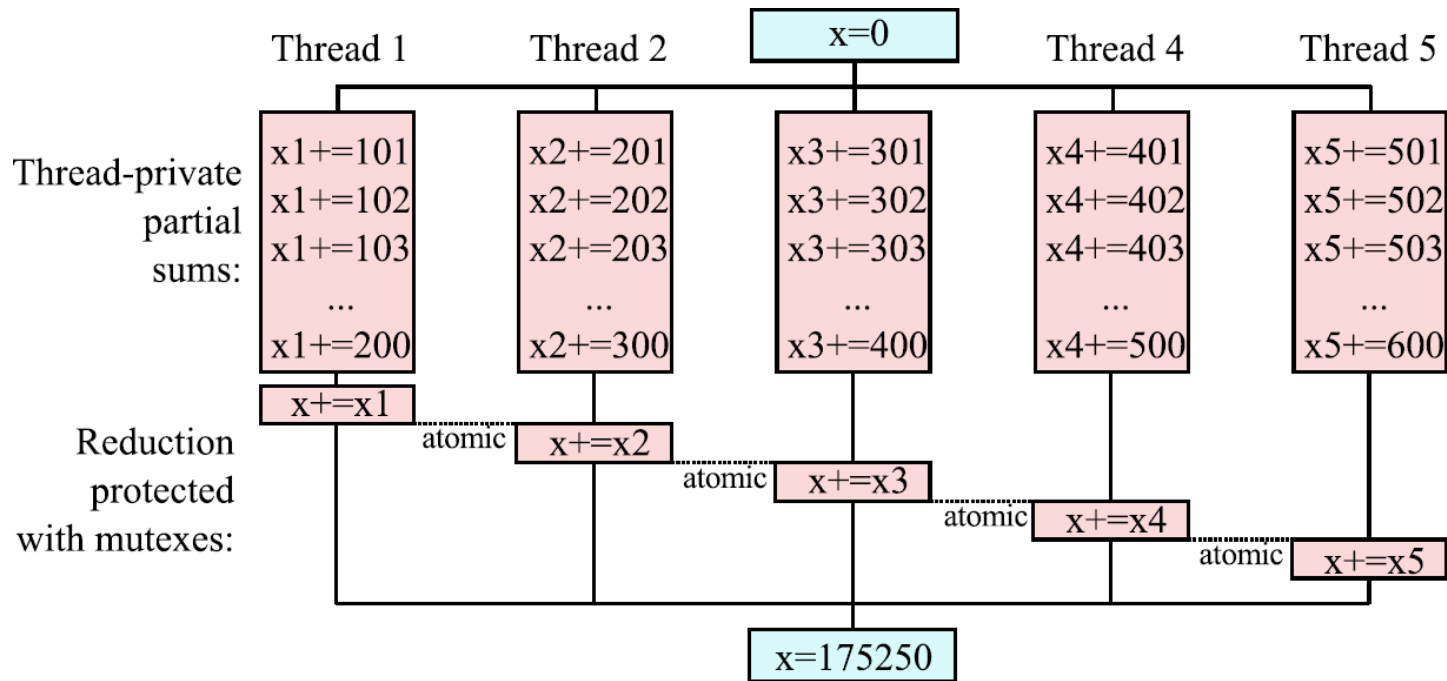
DATA RACES



Race Condition!



PARALLEL REDUCTION



Key: using thread-private containers for partial sums; mutexes only after the parallel loop

OPTIMIZED VERSION

```
void BinParticles_2(const InputDataType& inputData, BinsType& outputBins){
#pragma omp parallel
    { BinsType threadPrivateBins; // Declare thread-private containers
      for (int i = 0; i < nBinsX; i++)
        for (int j = 0; j < nBinsY; j++)
          threadPrivateBins[i][j] = 0;
#pragma omp for
      for (int i = 0; i < inputData.numDataPoints; i++) {
        // ...transforming from cylindrical to Cartesian coordinates:
        // ...calculating the bin numbers for these coordinates:
        // Incrementing the appropriate bin in the thread-private counter:
        threadPrivateBins[iX][iY]++;
      }
      for(int i = 0; i < nBinsX; i++) // Reduction outside the parallel loop
        for(int j = 0; j < nBinsY; j++)
#pragma omp atomic
          outputBins[i][j] += threadPrivateBins[i][j];
    } }
```

THREAD AFFINITY

Threads:

0

1

2

3

4

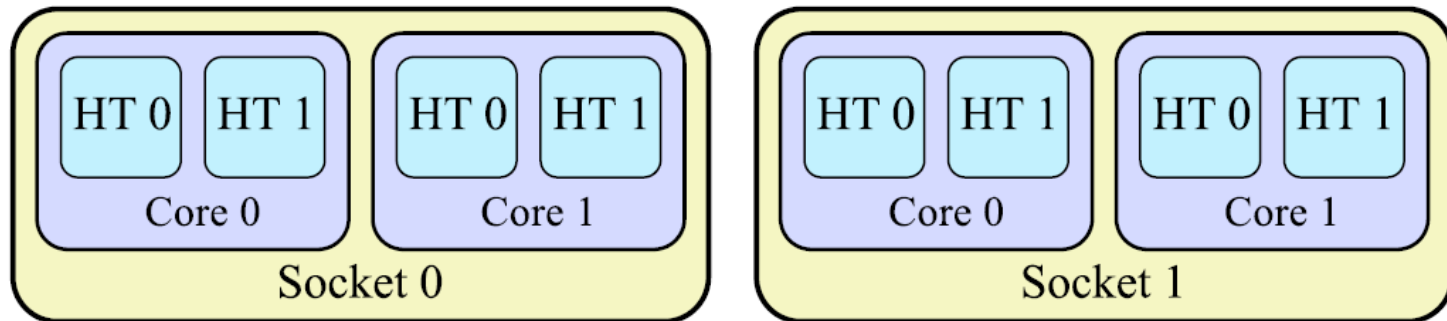
5

6

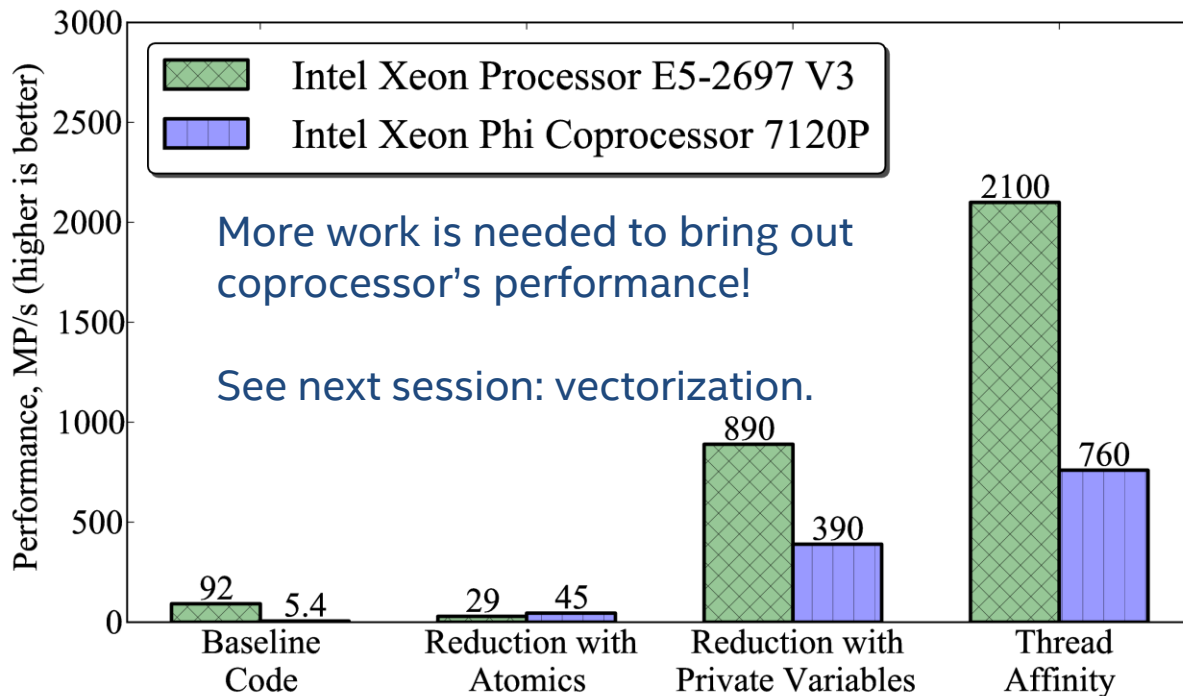
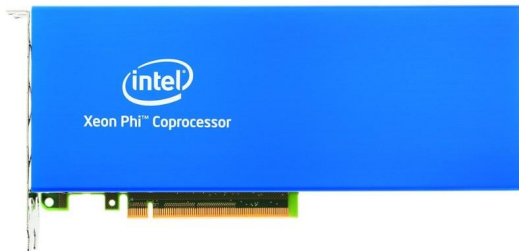
7



Cores:



PERFORMANCE RESULTS



NEXT SESSION

- Part 2: vectorization – another level of parallelism
- Part 3: making the memory subsystem happy

By the way:
download this tutorial
colfaxresearch.com



The screenshot shows the Colfax Research website. At the top, there is a navigation bar with links for READ, WATCH, LEARN, CONNECT, and JOIN. Below this is a diagram of a dual-core system. Core 0 contains Thread 0 and a Cache. Core 1 contains Thread 1 and a Cache. A shared Cache Line connects the two caches. Below the diagram is a title: "Optimization Techniques for the Intel MIC Architecture. Part 3 of 3: False Sharing and Padding".

The website also features several sections:

- Research and Educational Publications:** Includes "Introduction to Intel DAAL, Part 1: Polynomial Regression with Batch Mode Computation" and "Optimization Techniques for the Intel MIC Architecture. Part 3 of 3: False Sharing and Padding".
- Events:** Lists "Syllabus: Hands-On Workshop, November 2015" and "Archive: Hands-On Workshop, October 2015".
- Presentations:** Includes "The Hands-On Workshop (HOW) Series" and "Scientific Computing with Intel Xeon Phi Coprocessors".
- Services:** Offers "Face-to-face training on parallel programming, Intel architecture" and "Web-based hands-on training with remote access".